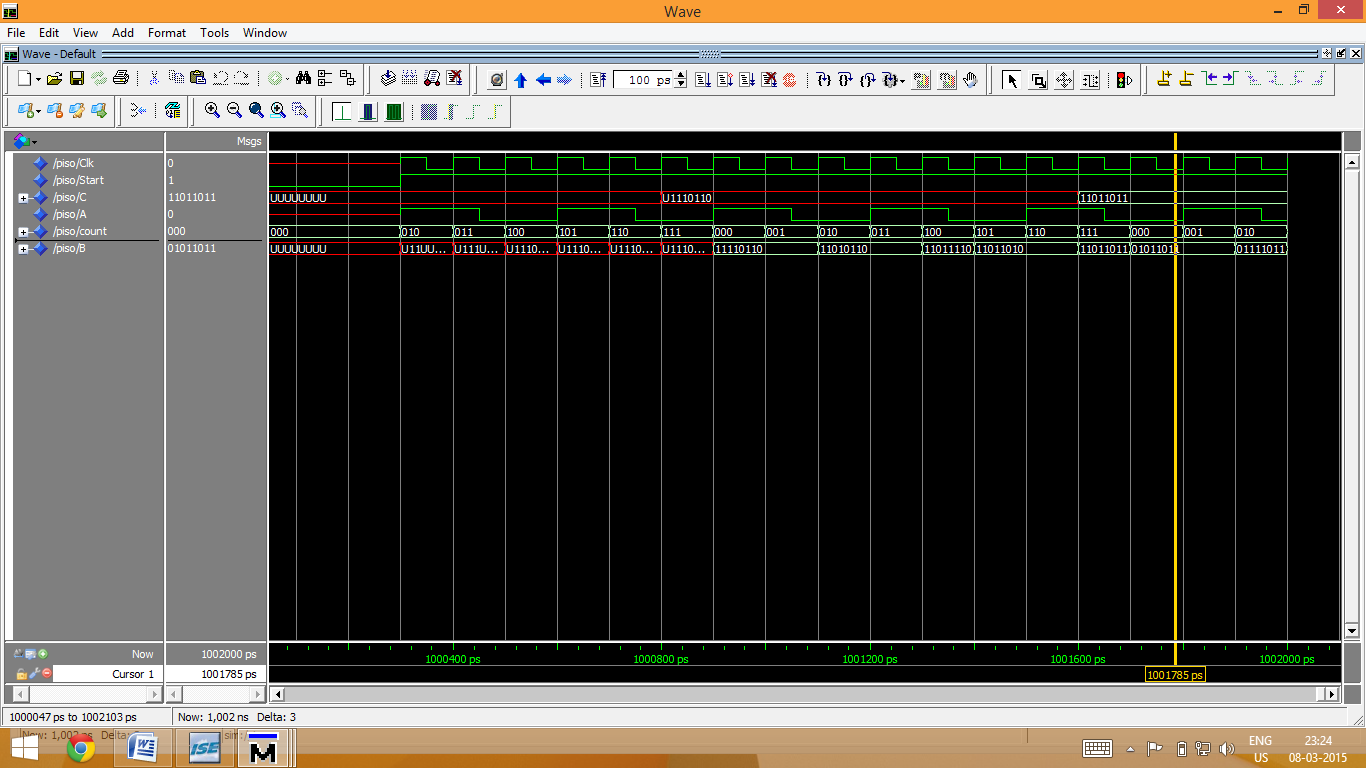
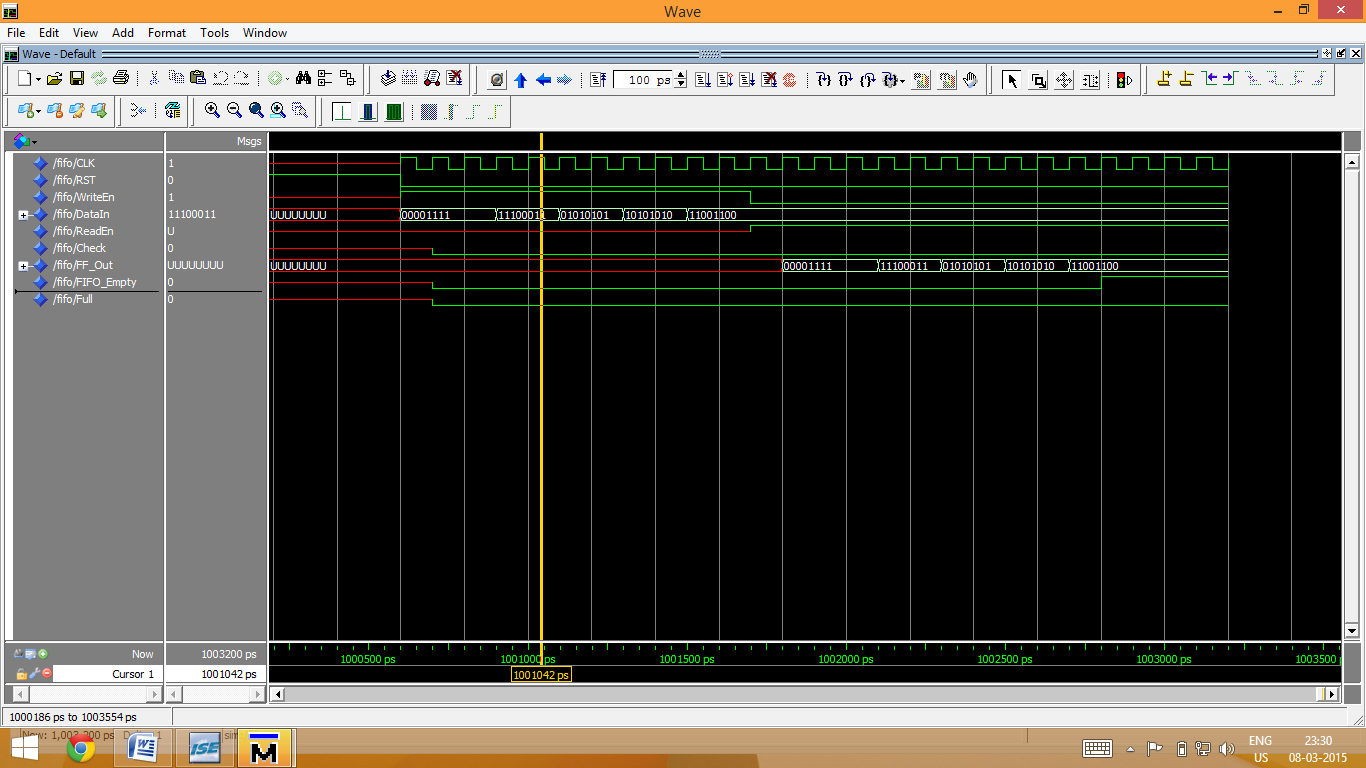
the simulation result of Parallel in Serial out in which 8 bit input is converted into single bit.

***Figure 3.1 PISO Result***

Figure 3.2 shows the simulation result of Serial in Parallel out in which 1 bit input is converted into 8 bit Data.

***Figure 3.1 SIPO Result***

Figure 3.3 shows the simulation result of FIFO when u make Write data make Wr High read data RD make High.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*